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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,064	11/21/2001	Ashley Saulsbury	016747-015500US	4869

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 04/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,064	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 01/27/2006.

2. Claims 1-21 are pending in this application. Claims 1, 8, and 18 are independent claims. In Amendment, claims 1, 8, and 18 are amended. This Office Action is made final.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Sijstermans et al. (U.S. 6,889,242).

Re claim 1, Sijstermans et al. disclose in Figures 1-2 and 4 a method for averaging two pixel values (e.g. abstract, Figure 4, and claim 2 in col. 15), comprising: decoding a single machine code instruction (e.g. 18 in Figure 1) comprising an address for a first input register, an address for a second input register, an address for an output register (e.g. col. 3 lines 45-53), an op code indicating a function to perform (e.g. as a functional code by unit 14 in Figure 1 and col. 3 lines 45-66), and a rounding factor (e.g. 202 in Figure 2 and col. 4 line 55 to col. 5 line 45); loading a plurality of first operands

from a first input register (e.g. rsrc1 as vectors in col. 6 lines 40-50); loading a plurality of second operands from a second input register (e.g. rsrc2 as vectors in col. 6 lines 40-50); producing an average, based on the op code, of one of the plurality of first operands and one of the plurality of second operands (e.g. output of Figure 4 after the right shifting and claims 1-2 in col. 15), wherein the rounding factor indicates which of a plurality of rounding algorithms to use in producing the average (e.g. col. 6 liens 55-65 and table 1 in col. 5), the plurality of rounding algorithms comprising: a first rounding algorithm able to produce a change in the average (e.g. depending on the rounding mode as seen in col. 5 lines 1-15); and a second rounding algorithm able to produce a change in the average (e.g. depending on the rounding mode as seen in col. 5 lines 1-15); and storing the average in an output register (e.g. rdest as vectors in col. 6 lines 40-50).

Re claim 2, Sijstermans et al. further disclose in Figures 1-2 and 4 determining how many fields are in each of the first and second input registers (e.g. col. 5 line 65 to col. 6 lines 55).

Re claim 3, Sijstermans et al. further disclose in Figures 1-2 and 4 the producing the average comprises: producing a first intermediate result by adding one of the plurality of first operands to one of the plurality of second operands (e.g. 402 in Figure 4); and producing the average by shifting the first intermediate result to the right by one binary digit (e.g. 404 in Figure 4).

Re claim 4, Sijstermans et al. further disclose in Figures 1-2 and 4 the producing the average comprises: producing a first intermediate result by adding one of the plurality of first operands, one of the plurality of second operands and the rounding factor (e.g.

402 and 406 in Figure 4); and producing the average by shifting the first intermediate result to the right by one binary digit (e.g. 404 in Figure 4).

Re claim 5, Sijstermans et al. further disclose in Figures 1-2 and 4 rounding the average before storing the average (e.g. rounding in 402-404 before output the results as rdest).

Re claim 6, Sijstermans et al. further disclose in Figures 1-2 and 4 evaluating the rounding factor, and adding a value to the average (e.g. col. 1 lines 1-45 and particularly table 1).

Re claim 7, Sijstermans et al. further disclose in Figures 1-2 and 4 the value is one of zero and one (e.g. 406 in Figure 4 and col. 5 lines 1-45).

Re claim 8, it has similar limitations cited in claim 1. Thus, claim 8 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 9, Sijstermans et al. further disclose in Figures 1-2 and 4 the instruction is one of a plurality of instructions in a long instruction word (e.g. col. 6 line 47 as VLIW).

Re claim 10, it has same limitations cited in claim 2. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 11, it has same limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it has same limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it has same limitations cited in claim 6. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 14, it has same limitations cited in claim 7. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 15, the first input register comprises a plurality of fields.

Re claim 16, it has same limitations cited in claim 5. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 17, Sijstermans et al. further disclose in Figures 1-2 and 4 loading a third operand from an A2 field of the first input register; loading a fourth operand from a B2 field of the second input register; producing a second average of the third operand and the fourth operand, and storing the second average in a C2 field of the output register (e.g. additional process of averaging step as seen in Figure 4 and col. 6 line 40 to col. 7 line 15).

Re claim 18, it is an apparatus claim of claim 1. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 19, Sijstermans et al. further disclose in Figures 1-2 and 4 average module comprises: a plurality of adders respectively coupled to the first and second fields (e.g. inherently for adding vectors as seen in Figure 4); and a plurality of shifters respectively coupled to the plurality of adders (e.g. inherently for shifting vectors as seen in Figure 4).

Re claim 20, Sijstermans et al. further disclose in Figures 1-2 and 4 the rounding factor causes at least one of rounding-up or rounding-down by the plurality of average modules (e.g. col. 5 lines 1-15).

Re claim 21, Sijstermans et al. further disclose in Figures 1-2 and 4 the rounding factor is added to the first and second fields in the average module (e.g. 406 in Figure 4 and col. 5 lines 1-45).

Response to Arguments

5. Applicant's arguments filed 01/27/2006 have been fully considered but they are not persuasive.

a. The applicant argues in page 11 first and second paragraphs for claim 1 that the cited reference fails to disclose the machine code instruction comprising an address for the first input register, an address for the second input register, an address for the output register, the op code indicating a function to perform, and the rounding factor as cited in the claim.

The examiner respectfully submits that the cited reference clearly discloses VLIW instruction capable of including plurality of instruction slots wherein each slot may be adapted to executed one operation (e.g. col. 3 lines 55-68). Further more, the cited reference also clearly indicated an instruction with addresses of source(s) and destination for fetching and storing the operands (e.g. col. 3 lines 45-53 and col. 6 lines 1-40). The op code is the main code within the instruction as averaging which is symbolized as avg4_bu as an example in column 6 lines 1-40

and founding factor is also included in the instruction, which executed according to the control register 22 (e.g. col. 3 lines 45-53). Clearly, the VLIW instruction is considered as a single instruction which includes multiple instructions for performing sub-operations. The avg4_bu is not an syntax but it is rather an opcode within the instruction for telling the decoder how to execute the instruction.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

April 11, 2006

JOHN CHAVIS
PATENT EXAMINER
ART UNIT 2193